Docket No. 10001846-1
USPTO Ser. No. 09/659,256

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Matter of the Application of: Alan Krech et al.
Serial No. : 09/659,256
Filed: September 11, 2000
For : Method and Apparatus for No-latency Conditional Branching
Examiner: Shrader
Group Art Unit: 2124

#3
S. Cottrell
6-5-03

Assistant Commissioner for Patents
Washington, DC 20231

Response to Outstanding Office Action

Dear Sir,

Remarks

Office Action dated March 31, 2003 rejects all claims. In response, all claims remain unamended, the rejections are respectfully traversed, and consideration of the following Remarks is respectfully requested.

Claim 1 is rejected as rendered obvious by US Pat. No. 5,991,868 to Kamiyama (herein "the Kamiyama patent") in view of US Pat. No. 5,740,393 to Vidwans (herein "the Vidwans patent"). Specifically, the Office Action suggests that the Kamiyama patent teaches conditional branching with a flag used to determine if a branch is to occur and the Vidwans patent (Figure 9) teaches first and second sets of multiplexors to create a single flag bit as an output. With all due respects, Applicant believes that Figure 9 of the Vidwans patent and accompanying disclosure teaches an instruction pointer logic circuit that results in a multiple bit value that is transferred to an